In the Claims:

1. (Currently Amended) A non-volatile memory device comprising:

a substrate having a plurality of isolation layers and a plurality of active regions therebetween;

~~a plurality of isolation layers on the substrate that define a plurality of active regions therebetween;~~

a charge storage insulator covering ~~on~~ the plurality of active regions and the plurality of isolation layers; and

a plurality of gate lines on the charge storage insulator ~~and crossing over the plurality of active regions~~.

2. (Currently Amended) The non-volatile memory device of Claim [[40]] 1, wherein a top surface of each of the plurality of isolation layers is disposed farther above the substrate than a top surface of each of the plurality of active regions.

3. (Currently Amended) The non-volatile memory device of Claim [[40]], wherein the charge storage insulator comprises a multi-layer structure having at least one oxide layer.

4. (Currently Amended) The non-volatile memory device of Claim [[3]] 1, wherein ~~at least one of the at least one oxide layers~~ the charge storage insulating layer comprises at least one ~~an~~ insulating metal oxide layer.

5. (Currently Amended) The non-volatile memory device of Claim [[40]] 1, wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer disposed on the lower oxide layer and an insulating metal oxide layer disposed on the charge trapping layer.

6. (Canceled)

7. (Currently Amended) A non-volatile memory device comprising:

a substrate having a cell region, a high voltage region and a low voltage region;

a plurality of trench isolation layers on the substrate that define a plurality of first active regions in the cell region, a plurality of second active regions in the high voltage region and a plurality of third active regions in the low voltage region;

a charge storage insulator on the plurality of first active regions and the plurality of trench isolation layers in the cell region of the device;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of first active regions and the plurality of trench isolation layers in the cell region ~~of the device~~.

8. (Currently Amended) The non-volatile memory device of Claim 7, the device further comprising:

a high voltage gate electrode crossing over each of the plurality of second active regions and a first gate insulation layer interposed between the high voltage gate electrode and each of the plurality of second active regions.

a low voltage gate electrode crossing over each of the plurality of third active regions and a second gate insulation layer interposed between the low voltage gate electrode and each of the plurality of third active regions.

9. (Currently Amended) The non-volatile memory device of Claim 7, wherein a top surface of each of the plurality of trench isolation layers is higher ~~disposed farther above the substrate~~ than a top surface of each of the plurality of first, second and third active regions.

10. (Original) The non-volatile memory device of Claim 7, wherein the charge storage insulator is a multi-layer structure that includes an insulating metal oxide layer.

11. (Currently Amended) The non-volatile memory device of Claim 8, wherein the first gate insulation layer is thicker than the second gate insulation layer.

12. (Currently Amended) ~~The non-volatile memory device of Claim 11,~~ A non-volatile memory device comprising:

a substrate having a cell region;

a plurality of trench isolation layers that define a plurality of first active regions in the cell region, a plurality of second active regions in a high voltage region and a plurality of third active regions in a low voltage region;

a charge storage insulator on the plurality of first active regions and the plurality of trench isolation layers in the cell region;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of trench isolation layers in the cell region;

a high voltage gate electrode crossing over each of the plurality of second active regions and a first gate insulation layer interposed between the high voltage gate electrode and each of the plurality of second active regions; and

a low voltage gate electrode crossing over each of the plurality of third active regions and a second gate insulation layer interposed between the low voltage gate electrode and each of the plurality of third active regions;

wherein the first gate insulation layer is thicker than the second gate insulation layer; and

wherein the first gate insulation layer comprises a first oxide layer and a lower oxide layer and wherein the second gate insulation layer comprises a second oxide layer and a lower oxide layer.

13. (Currently Amended) The non-volatile memory device of Claim 12, wherein the plurality of gate lines include a plurality of word lines, a ground selection gate line and a string selection gate line and wherein the second oxide layer is further interposed between the charge storage insulator and the first active region ~~at the regions of the charge storage insulator that~~ are under the ground and string selection gate lines.

14. (Currently Amended) ~~The non-volatile memory device of Claim 8,~~ A non-volatile memory device comprising:

a substrate having a cell region;

a plurality of trench isolation layers on the substrate that define a plurality of first active regions in a cell region, a plurality of second active regions in a high voltage region and a plurality of third active regions in the low voltage region;

a charge storage insulator on the plurality of first active regions and the plurality of trench isolation layers in the cell region;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of trench isolation layers in the cell region;

a high voltage gate electrode crossing over each of the plurality of second active regions and a first gate insulation layer interposed between the high voltage gate electrode and each of the plurality of second active regions; and

a low voltage gate electrode crossing over each of the plurality of third active regions and a second gate insulation layer interposed between the low voltage gate electrode and each of the plurality of third active regions;

wherein the first gate insulation layer comprises a first oxide layer, a lower oxide layer and a second oxide layer and wherein the second gate insulation layer comprises the lower oxide layer and the second oxide layer.

15. (Original) The non-volatile memory device of Claim 14, wherein the first insulation layer and the second insulation layer each further comprise an upper oxide layer on the second oxide layer.

16. (Currently Amended) The non-volatile memory device of Claim 13, wherein the plurality of gate lines include a plurality of word lines, a ground selection gate line and a string selection gate line and wherein [[a]] the lower oxide layer is further interposed between the string selection gate line and the plurality of first active regions, and between the ground selection gate line and the plurality of first active regions.

17. (Currently Amended) ~~The non-volatile memory device of Claim 8,~~ A non-volatile memory device comprising:

a substrate having a cell region;

a plurality of trench isolation layers on the substrate that define a plurality of first active regions in the cell region, a plurality of second active regions in a high voltage region and a plurality of third active regions in a low voltage region;

a charge storage insulator on the plurality of first active regions and the plurality of trench isolation layers in the cell region;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of trench isolation layers in the cell region;

a high voltage gate electrode crossing over each of the plurality of second active regions and a first insulation layer interposed between the high voltage gate electrode and each of the plurality of second active regions; and

a low voltage gate electrode crossing over each of the plurality of third active regions and a second insulation layer interposed between the low voltage gate electrode and each of the plurality of third active regions;

wherein the first insulation layer comprises a first oxide layer and a second oxide layer and wherein the second insulation layer comprises the second oxide layer.

18. (Currently Amended) The non-volatile memory device of Claim 17, wherein each of the plurality of gate lines comprises a second conductive layer and a third conductive layer and wherein the high and low voltage gate electrodes comprise [[a]] the first conductive layer and [[a]] the third conductive layer.

19. (Currently Amended) A non-volatile memory device comprising:

a substrate having a cell region~~, a high voltage region and a low voltage region~~;

a plurality of device isolation layers ~~on the substrate~~ that define a plurality of first active regions in ~~the~~ a cell region, a second active region in ~~the~~ a high voltage region and a third active region in ~~the~~ a low voltage region;

a charge storage insulator disposed on the first active regions and the plurality of device isolation layers wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer and an upper oxide layer;

a plurality of gate lines on the charge storage insulator ~~that cross over the plurality of device isolation layers~~;

a first gate electrode crossing over the second active region;

a second gate electrode crossing over the third active region;

a first gate insulation layer interposed between the first gate electrode and the second active region; and

a second gate insulation layer interposed between the second gate electrode and the third active region.

20. (Original) The non-volatile memory device of Claim 19, wherein the plurality of gate lines include a plurality of word lines disposed in a word line portion of the cell region, and a ground selection gate line and a string selection gate line that are disposed in a selection gate portion of the cell region and wherein the lower oxide layer of the charge storage insulator is thinner under the plurality of word lines than the lower oxide layer of the charge storage insulator is under the ground selection gate line and the string selection gate line.

21-39. (Canceled).

40. (Currently Amended) ~~The non-volatile memory device of Claim 1,~~ A non-volatile memory device comprising:

a substrate having a plurality of isolation layers and a plurality of active regions therebetween;

a charge storage insulator on the plurality of active regions and the plurality of isolation layers;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of active regions; and

~~further comprising~~ a plurality of conductive patterns disposed between at least some of the gate lines that penetrate the charge storage insulator to electrically connect with at least some of the plurality of active regions.

41. (New) The non-volatile memory device of Claim 40, wherein a top surface of each of the plurality of isolation layers is disposed farther above the substrate than a top surface of each of the plurality of active regions.

42. (New) The non-volatile memory device of Claim 40, wherein the charge storage insulator comprises a multi-layer structure having at least one oxide layer.

43. (New) The non-volatile memory device of Claim 40, wherein the charge storage insulator comprises at least one insulating metal oxide layer.

44. (New) The non-volatile memory device of Claim 40, wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer disposed on the lower oxide layer and an insulating metal oxide layer disposed on the charge trapping layer.

45. (New) The non-volatile memory device of Claim 40, wherein the plurality of isolation layers and the plurality of active regions are located in a cell region of the device and wherein the charge storage insulator is on substantially the entire surface of the cell region.

46. (New) A non-volatile memory device comprising:

a substrate having a plurality of isolation layers and a plurality of active regions therebetween;

a charge storage insulator on the plurality of active regions and the plurality of isolation layers;

wherein the charge storage insulator comprises a multi-layer structure having at least one insulating metal oxide layer; and

a plurality of gate lines on the charge storage insulator and crossing over the plurality of active regions.

47. (New) The non-volatile memory device of Claim 46, wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer disposed on the lower oxide layer and an insulating metal oxide layer disposed on the charge trapping layer.

48. (New) The non-volatile memory device of Claim 47, wherein the lower oxide layer comprises an insulating metal oxide layer.

49. (New) The non-volatile memory device of Claim 12, wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer disposed on the lower oxide layer and an upper oxide layer disposed on the charge trapping layer.

50 (New) The non-volatile memory device of Claim 15, wherein the charge storage insulator comprises the lower oxide layer, a charge trapping layer disposed on the lower oxide layer and the upper oxide layer disposed on the charge trapping layer.

51. (New) The non-volatile memory device of Claim 19, wherein the upper oxide layer comprises an insulating metal oxide layer.

52. (New) The non-volatile memory device of Claim 19, wherein the lower oxide layer comprises an insulating metal oxide layer.

53. (New)) The non-volatile memory device of Claim 19, wherein the first gate insulation layer is thicker than the second gate insulation layer.